

CLAIMS

What is claimed is:

1. A near-unity divider apparatus in a direct conversion communication
 5 device, the divider comprising:
 - a reference frequency output from a frequency source;
 - a multiply-by-two circuit that doubles the reference frequency and outputs the
 doubled frequency;
 - a divide-by-three circuit coupled to the multiply-by-two circuit, the divide-by-three
 10 circuit divides the doubled frequency by three to output a first fractionally-divided
 frequency;
 - a delay generator coupled to the divide-by-three circuit, the delay generator inputs
 the first fractionally-divided frequency from the divide-by-three circuit and provides a
 second fractionally-divided frequency shifted a predetermined time period; and
 - 15 a gate circuit that combines the first and second fractionally-divided frequencies to
 provide a fractionally-divided frequency with an adjustable duty cycle dependant upon the
 predetermined time period.

2. The apparatus of claim 1, wherein the delay generator is coupled to the multiply-by-two circuit, wherein the delay generator uses the doubled frequency as a clock.

5 3. The apparatus of claim 1, wherein the delay generator is coupled to the multiply-by-two circuit, wherein the delay generator uses the doubled frequency as a clock, and the predetermined time period is one half clock cycle such that the duty cycle is fifty-percent.

10 4. The apparatus of claim 1, wherein the gate circuit is an AND gate.

5. The apparatus of claim 1, wherein the delay circuit is a D-type flip-flop.

15 6. The apparatus of claim 1, further comprising a switchable frequency doubler coupled in the divider, wherein the frequency doubler switchably doubles the operating frequencies of the apparatus.

20 7. The apparatus of claim 1, wherein the first fractionally-divided frequency has a two-thirds duty cycle.

8. A direct conversion radio communication apparatus with a near-unity divider for limiting on-channel frequencies, the apparatus comprising:

a reference frequency output from a frequency source;

5 a multiply-by-two circuit that doubles the reference frequency and outputs the doubled frequency;

a divide-by-three circuit coupled to the multiply-by-two circuit, the divide-by-three circuit divides the doubled frequency by three to output a first fractionally-divided frequency;

10 a delay generator coupled to the multiply-by-two circuit and the divide-by-three circuit, the delay generator uses the doubled frequency from the multiply-by-two circuit as a clock and inputs the first fractionally-divided frequency from the divide-by-three circuit to provide a second fractionally-divided frequency delayed a predetermined time period; and

15 an AND gate circuit that combines the first and second fractionally-divided frequencies to provide a fractionally-divided frequency with an adjustable duty cycle dependant upon the predetermined time period.

9. The apparatus of claim 8, wherein the predetermined time period is one half clock cycle such that the duty cycle is fifty-percent.

10. The apparatus of claim 8, wherein the delay circuit is a D-type flip-flop.

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11. The apparatus of claim 8, further comprising a switchable frequency doubler coupled in the divider, wherein the frequency doubler doubles the operating frequencies of the apparatus.

10 12. The apparatus of claim 8, wherein the first fractionally-divided frequency has a two-thirds duty cycle.

13. A method of limiting on-channel frequencies in a direct conversion communication device, the method comprising the steps of:

receiving a reference frequency from a frequency source;

doubling the reference frequency to provide a first doubled frequency;

5 dividing the first doubled frequency by three to provide a first fractionally-divided frequency;

shifting the first fractionally-divided frequency to provide a second fractionally-divided frequency; and

10 gating the first and second fractionally-divided frequencies to provide a fractionally-divided frequency with an adjustable duty cycle dependant upon the predetermined time period.

14. The method of claim 13, wherein the shifting step includes clocking the first fractionally-divided frequency with the first doubled frequency.

5 15. The method of claim 13, wherein the dividing step provides a first fractionally-divided frequency with a two-thirds duty cycle.

16. The method of claim 13, wherein the gating step uses AND gating.

10 17. The method of claim 13, wherein the shifting step uses a D-type flip-flop.

18. The method of claim 13, further comprising a step of providing a switchable frequency doubler for switchably doubling the reference frequency from the frequency source.

15 19. The method of claim 13, wherein the shifting step includes clocking the first fractionally-divided frequency with the first doubled frequency and shifting the second fractionally-divided frequency by one-half clock cycle such that the gating step provides a duty cycle of fifty-percent.

20 20. The method of claim 19, wherein the shifting step includes delaying the second fractionally-divided frequency by one-half clock cycle.